

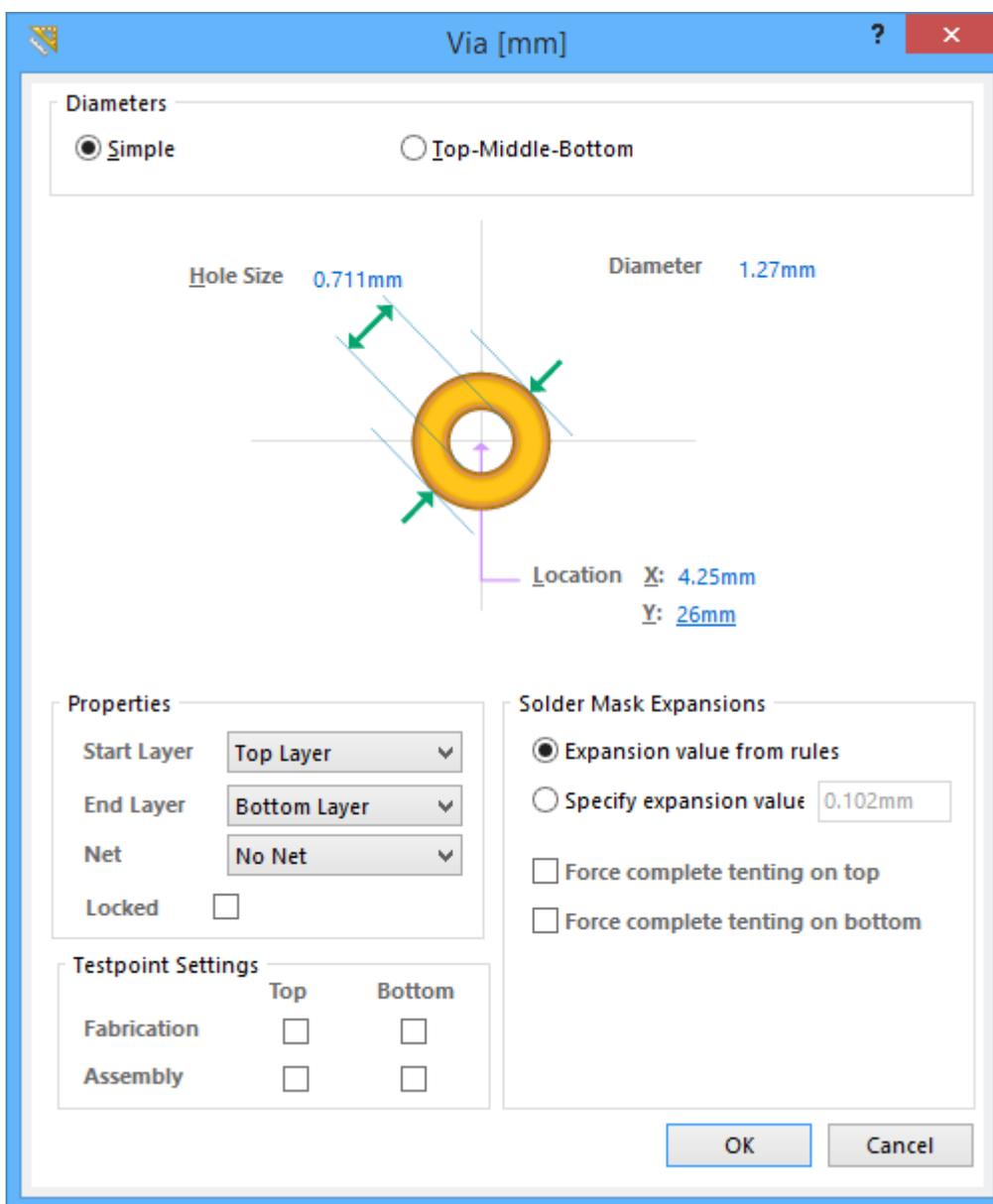
Via

Modified by Annika Krilov on Jun 24, 2015

Other Related Resources

[Via \(Object\)](#)

Parent page: [PCB Dialogs](#)



The Via Dialog.

Summary

The *Via* dialog allows the designer to edit the properties of a Via. A via is used to create vertical connections between the signal layers of a PCB. A via has a hole, that once it is plated, creates this vertical connectivity. Vias can span all layers in the board design, or can start and stop at specific layers. Note that these types of vias can only be designed in conjunction with the board fabricator, as they must have the appropriate processes and technology to create vias between the specified layers.

Access

The *Via* dialog can be accessed prior to entering placement mode, from the **PCB Editor - Defaults** page of the *Preferences* dialog (**File | Preferences**). This allows you to change the default properties for the via object, which will be applied when placing subsequent vias.

This dialog can be accessed during placement by pressing the **TAB** key.

After placement, the dialog can be accessed in the following ways:

- Double-click on the placed object.
- Place the cursor over the object, right-click and choose **Properties** from the context menu.

Options/Controls

Diameters

- **Simple** - The via Diameter is the same on all layers.
 - **Diameter** - Specify the diameter of the via.
- **Top-Middle-Bottom** - Different Diameters can be set for the: Top Layer, all internal signal layers, and Bottom Layer respectively.
 - **Top Layer** - Specify the via diameter for the Top Layer.
 - **Middle Layer** - Specify the via diameter for the Middle layers (all internal signal layers).
 - **Bottom Layer** - Specify the via diameter for the Bottom layer.
- **Hole size** - The size of the hole in the via.
- **Location X/Y** - The X and Y coordinates of the via.

Properties

- **Start Layer** - The layer that this via starts on.
- **End Layer** - The layer that this via ends on.
- **Net** - The net that the via is currently assigned to. Change the net assignment by clicking in the field and choosing a net from the drop down list. Select **No Net** to specify that the via is not connected to any net. The Net property of a primitive is used by the Design Rule Checker to determine if a PCB object is legally placed.
- **Locked** - Enable this option to protect the via from being edited graphically. Lock a via whose position is critical. If you try to edit a primitive that is locked, you will be informed that the primitive is locked and asked if you wish to proceed with the action. If this option is unchecked, the primitive can be freely edited without confirmation.



The **Start Layer** and **End Layer** settings define a via to be one of the following types:

- **Multi-layer (Thru-Hole)** - this type of via passes from the Top layer to the Bottom layer and allows connections to all internal signal layers.
- **Blind** - this type of via connects from the surface of the board to an internal electrical layer.
- **Buried** - this type of via connects from one internal electrical layer to another internal electrical layer.

Testpoint Settings

Use the Testpoint Settings to define this via as a testpoint for **Fabrication** and/or **Assembly** testpoint file generation. A testpoint is a location where a test probe can make contact with the PCB to check for correct function of the board. Any via or via can be nominated as a testpoint, when this is done the component that the via or via belongs to, automatically gets locked. Separate Fabrication and Assembly Testpoint files are generated from the **Outputs** tab of the Ribbon.

- **Top** - Enable this option for this via to be defined as a top layer testpoint.
- **Bottom** - Enable this option for this via to be defined as a bottom layer testpoint.

Solder Mask Expansions

An opening in the solder mask is automatically created by the software, the same shape as the via. This opening can be larger (a positive expansion value) or smaller (a negative expansion value) than the via itself, as defined by the Solder Mask Expansion setting. The expansion is measured from the edge of the copper.

- **Expansion value from rules** - When this option is enabled the solder mask expansion for this pad is defined by the applicable [Solder Mask Expansion](#) design rule.
- **Specify expansion value** - Enable this option to override the rule and specify the solder mask expansion value for this pad.
- **Force complete tenting on top** - The term tenting means *to close off*. If this option is enabled then the settings in the applicable solder mask expansion design rule will be overridden, resulting in no opening in the solder mask on the top solder mask layer for this pad. When this option is enabled, the **Expansion value from rules** and the **Specify expansion value** options are ignored.
- **Force complete tenting on bottom** - The term tenting means *to close off*. If this option is enabled then the settings in the applicable solder mask expansion design rule will be overridden, resulting in no opening in the solder mask on the bottom solder mask layer for this pad. When this option is enabled, the **Expansion value from rules** and the **Specify expansion value** options are ignored.

Tenting

Partial and complete tenting of vias can also be achieved by defining an appropriate value for Solder Mask Expansion. This expansion constraint can either be defined on a via-by-via basis in the associated *Via* dialog, or by defining appropriate Solder Mask Expansion design rules. By setting the expansion value to a suitable value, you can achieve the following:

- To partially tent a via - covering the land area only, set the Expansion to a negative value that will close the mask right up to the via hole.
- To completely tent a via - covering the land and hole, set the Expansion to a negative value

equal to or greater than the via radius.

- To tent all vias on a single layer, set the appropriate Expansion value and ensure that the scope (Full Query) of a Solder Mask Expansion rule targets all vias on the required layer.
- To completely tent all vias in a design, in which varying via sizes are defined, set the Expansion to a negative value equal to or greater than the largest via radius.

When tenting an individual via, options are available to follow the expansion defined in the applicable design rule, or to override the rule and apply a specified expansion directly to the individual via in question.

Source URL: [http://documentation.circuitmaker.com/display/CMAK/PCB_Dlg-Via\(\(Via\)\)_CM](http://documentation.circuitmaker.com/display/CMAK/PCB_Dlg-Via((Via))_CM)