


Mismatched Pin Visibility

Modified by Jason Howie on Oct 20, 2014

Parent category: [Violations Associated with Components](#)

Default report mode:  Error

Summary

This violation is related to the power pins (VCC and GND) of a multi-part component. Typically, these pins are associated to part 0, are automatically connected to the VCC and GND nets for the design, and are hidden. If, for one of the component parts, you enable visibility of such a pin, it is no longer connected to the target power net and the error will be flagged.

Notification

If compiler errors and warnings are enabled for display on the schematic (enabled on the **Schematic - Compiler** page of the *Preferences* dialog) an offending object will display a colored squiggle beneath it. A notification is also displayed in the *Messages* panel in the following format:

Pin is visible in one sub-part and hidden in another sub-part

Recommendation for Resolution

Either disable display of the offending power pin(s) in the workspace or, if keeping the pins displayed, ensure that a VCC and/or GND power port object is attached to the pin(s) accordingly.

Source URL:

[http://documentation.circuitmaker.com/display/CMAK/WorkspaceManager_Err-MismatchedPinVisibility\(\(Mismatched+Pin+Visibility\)\)_CM](http://documentation.circuitmaker.com/display/CMAK/WorkspaceManager_Err-MismatchedPinVisibility((Mismatched+Pin+Visibility))_CM)