


## Mismatched Bus or Wire Object on Wire or Bus

Modified by Jason Howie on Oct 20, 2014

Parent category: [Violations Associated with Buses](#)

Default report mode:  Error

### Summary

This violation occurs when a wire object is incorrectly connected to a bus, or a bus object is incorrectly connected to a wire. For example a port, A, might be connected to a bus, but the correct bus label syntax (e.g. A[0..1]) has not been entered for the port's name. In effect, the port is a single signal (or wire) object that is now erroneously connected to a bus.

### Notification

If compiler errors and warnings are enabled for display on the schematic (enabled on the **Schematic - Compiler** page of the *Preferences* dialog) an offending object will display a colored squiggle beneath it. A notification is also displayed in the *Messages* panel in the following format:

*<ObjectIdentifier>* at *<Location>* placed on a *<ObjectType>*,

where:

*ObjectIdentifier* represents the mismatched object, which can be either a bus or wire object (e.g. pin, port, power port, net label, off-sheet connector, sheet entry). The identifier will appear in one of the following two formats:

- For a bus - Bus *<Object>* *<Name>* (e.g. Bus Net Label GND\_BUS[.]).
- For a wire - Wire *<Object>* *<Name>* (e.g. Wire Port TXD).

*Location* is the X,Y coordinates for the object's electrical hotspot.

*ObjectType* is the object on which the offending object has been placed - either a wire or a bus.

### Recommendation for Resolution

With the violation selected in the *Messages* panel, use the **Details** region of the panel to quickly cross probe to the offending object. To resolve the issue, consider the following:

- *Is the connection correct?* - should a bus connecting to the object really be a wire and vice versa.
- *Is the object defined correctly?* - for a bus object, ensure that the object's name is specified using the correct bus syntax, in the form *<Name>*[*<LowIndex>*..*<HighIndex>*] or *<Name>*[*<HighIndex>*..*<LowIndex>*]. For example a byte-wide data output port might be

specified as DAT\_OUT[7..0]. For a wire object, ensure that the object's name defines a single signal and is not defined using bus syntax.

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**Source URL:**

[http://documentation.circuitmaker.com/display/CMAK/WorkspaceManager\\_Err-MismatchedBusWireObjectOnWireBus\(\(Mismatched+Bus+or+Wire+Object+on+Wire+or+Bus\)\)\\_CM](http://documentation.circuitmaker.com/display/CMAK/WorkspaceManager_Err-MismatchedBusWireObjectOnWireBus((Mismatched+Bus+or+Wire+Object+on+Wire+or+Bus))_CM)