Mismatched Bus Widths

Modified by Jason Howie on Oct 20, 2014

Parent category: Violations Associated with Buses

Default report mode: Warning

Summary

This violation occurs when two net identifiers associated with the same bus slice define bus labels with differing widths. For example, a port, with name `A[0..7]`, might be connected to a bus whose attached net label is defined as `A[0..15]`.

Notification

If compiler errors and warnings are enabled for display on the schematic (enabled on the **Schematic - Compiler** page of the *Preferences* dialog) an offending object will display a colored squiggle beneath it. A notification is also displayed in the *Messages* panel in the following format:

`Mismatched bus widths on bus section <NetName> (<BusSize1> and <BusSize2>),`

where:

NetName is the name of the parent net to which the mismatched bus objects are associated.

BusSize1 is the width of the first of the offending bus objects.

BusSize2 is the width of the second of the offending bus objects.

Recommendation for Resolution

With the violation selected in the *Messages* panel, use the **Details** region of the panel to quickly trace the affected bus slice and identify the net identifiers (port, net label, sheet entry etc), the bus label widths of which are not consistent. Determine the correct width and amend the naming for the erroneous object.