Mismatched Bus Label Ordering

Modified by Jason Howie on Oct 20, 2014

Parent category: Violations Associated with Buses

Default report mode: Warning

Summary

This violation occurs when two net identifiers associated with the same bus slice define bus labels with ordering that is not in the same direction (ascending or descending).

Notification

If compiler errors and warnings are enabled for display on the schematic (enabled on the **Schematic - Compiler** page of the *Preferences* dialog) an offending object will display a colored squiggle beneath it. A notification is also displayed in the *Messages* panel in the following format:

`Mismatched bus ordering on <NetName> Low value first and High value first ,`

where

NetName is the name of the parent net to which the mismatched bus ordering is associated.

Recommendation for Resolution

With the violation selected in the *Messages* panel, use the **Details** region of the panel to quickly trace the affected bus slice and identify the net identifiers (port, net label, sheet entry, etc) whose bus ordering is not consistent. Determine the correct ordering and amend the naming for the erroneous object.